#Microelectronics

Your PhD starts here!

Silicon Components Division 2026

Why integrate our research division?

Follow @CEA-Leti

Photo credit: P.JAYET/CEA

About CEA-Leti

Empowering global change through science, technology and semiconductor innovation for a better world

CEA-Leti, a technology research institute at CEA, is a global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions for industry. Founded in 1967, CEA-Leti pioneers micro-& nanotechnologies, tailoring differentiating applicative solutions for global companies, SMEs and startups.

CEA-Leti tackles critical challenges in healthcare, energy and digital migration. From sensors to data processing and computing solutions, CEA-Leti's multidisciplinary teams deliver solid expertise, leveraging world-class pre-industrialization facilities.

With a staff of more than 2,000, a portfolio of 3,200 patents, 14,000 sq. meters of cleanroom space and a clear IP policy, the institute is based in Grenoble, France, and has offices in Silicon Valley, Brussels and Tokyo.

CEA-Leti has launched 80 startups and is a member of the Carnot Institutes network.

Join CEA-Leti and benefit from:

- Resources to address major societal challenges
- Multidisciplinary networks to conduct your research
- World-class technological platforms
- An international scientific, high-skills environment
- The strength of a major public research organization

A global presence with offices in France, San Francisco, Brussels and Tokyo

€350
million annual operating budget

2,000 talents,
including 230 Ph.D. students

3,200
patents in portfolio

600
publications per years

14,000 sq.m
of cleanrooms

80
startups created

ISO 9001
certified since 2000

CEA-Leti, a Great Place for Your Internship!

A dynamic microelectronics environment

Grenoble, the French silicon valley with

1/4 of French jobs in electronics

+ 27 000 jobs in microelectronics

Cutting edge equipment:
A nanocharacterization platform with resources that are unique in the world, cleanrooms that is the only one of its kind in Europe, with a wide range of manufacturing processes.

- Cleanrooms platform
- Power electronics platform
- Integrated circuits design platform
- Microsystems 200 and 300mm platform
- Nanocharacterization platform

A vibrant, cosmopolitan metropolis open to the world, with an exceptional living environment

70 different nationalities in CEA-Grenoble

63 000 students, a university and schools with an international reputation

25 ski resorts close to the city

2 regional nature parks and 1 national park, breathtaking landscapes in all seasons and a wide range of outdoor activities

2 000 hours of sunshine a year

- Our unique microelectronics resources
- Our international reputation
- Our history
- Work and live in Grenoble
- PhD testimonies

Why Pursue a PhD in the Silicon Components Division?

Are you looking for the best path to kick-start your career as an engineer or researcher? We sat down with Gaël Pillonnet, Chief Scientist in the Silicon Components Division, to explore the exciting opportunities a PhD at CEA-Leti can offer.

What are the main benefits of doing a PhD in your division?

G.P.: "Pursuing a PhD in our division offers a unique and enriching experience. One of the best ways to understand the benefits is to ask our former PhD students! They often highlight four key advantages**"**:

1. **Personalized Mentorship**: Our PhD students receive dedicated guidance from experts, ensuring strong technical and professional growth.
2. **Cutting-Edge Research Environment**: Working with state-of-the-art technology enables students to push the boundaries of microelectronics research.
3. **Industry-Academia Balance**: The close proximity to industry offers both creative freedom and practical insights, ensuring that research remains impactful.
4. **Multidisciplinary Collaboration**: Students benefit from an ecosystem where physicists, chemists, engineers, and computer scientists work together, fostering innovation and teamwork."

What career opportunities are available after the PhD?

G.P.: "A PhD at CEA-Leti opens doors to both industry and academia. Many of our graduates join **top microelectronics companies** in France and abroad, leveraging our strong industrial collaborations. For those drawn to **academic research**, opportunities in universities and research labs remain a viable path. Additionally, the extensive **professional network** built during the PhD—spanning both industry and academia—helps guide career choices and create new opportunities."

What research topics can PhD students explore in your division?

G.P.: "Our division focuses on developing next-generation components for microelectronics, covering a broad range of research areas. PhD students might work on**"**:

1. **Fabrication & Characterization**: Exploring new materials and device architectures.
2. **Fundamental Understanding**: Investigating the physics behind component behavior.
3. **Simulation & Modeling**: Predicting performance and optimizing designs.
4. **Application Development**: Leveraging unique properties of components for real-world use cases."

What backgrounds are you looking for in PhD candidates?

G.P.: "We welcome a diverse range of profiles! While **microelectronics** is at our core, we also seek **chemists**, **physicists**, **computer scientists**, and **electronics** engineers. This diversity strengthens our teams, bringing together complementary expertise to tackle complex challenges in microelectronics."

Why Choose a PhD at CEA-Leti? Hear from Our Alumni!

Key numbers

100% of our doctors have published scientific articles

60% of our doctors have filed a patent during their thesis

40% of our doctors have had at least one internatial experience after their thesis

40% of our doctors work with an industrial partner

30% of our PhDs students are from abroad

25% have had an experience with a start-up

20% completed a “postdoctoral” fellowship at a research center

Based on PhD started between 2017 and 2019 in the Silicon Components Division

Loïck le Guevel

Academic experience: ENS Lyon, thesis defended in 2023

“ *I am currently working as an engineer at Google Quantum AI in Santa Barbara, California, where I am responsible for developing and testing next-generation control circuits for Google’s quantum computers. During my PhD, I had the privilege of working alongside renowned researchers in various areas of expertise within quantum computing. This stimulating environment, supported by the guidance of my supervisors, allowed me to not only deepen my technical skills but also gain international visibility, which has been crucial for my professional growth.*

“ ***The pros of CEA-Leti:*** *Interdisciplinary research, to have an international impact.*

Paola Trotti

Academic experience: Univ. di Pavia (Italy), thesis defended in 2022

“ *Currently an engineer at STMicroelectronics in Grenoble, I am involved in developing future generations of high-precision integrated circuits. My doctoral journey allowed me to fully engage in cutting-edge research on emerging memory technologies. I gained a wide range of skills, from electrochemistry to circuit design. This experience was further enriched by a scientific exchange in Germany, an opportunity that significantly broadened my PhD experience.*

“ ***The pros of CEA-Leti:*** *A stimulating research environment, exceptional mentoring, and the bonus of being close to the mountains!*

Adrien Morel

Academic experience: INSA Lyon, thesis defended in 2020

“ *Currently a lecturer at the University of Savoie Mont Blanc, I have chosen to pursue a career combining public research and teaching. Completing a PhD at the CEA was an invaluable opportunity, offering me a comfortable living environment and a scientific and technological setting conducive to creativity. The excellence of the supervision I received allowed me to successfully carry out my research project, exploring various approaches with complete freedom. This period was even more enriching as I had the chance to collaborate closely with engineers and PhD students, paving the way for innovative solutions and the emergence of new ideas.*

“ ***The pros of CEA-Leti:*** *Developing scientific skills in a stimulating environment!*

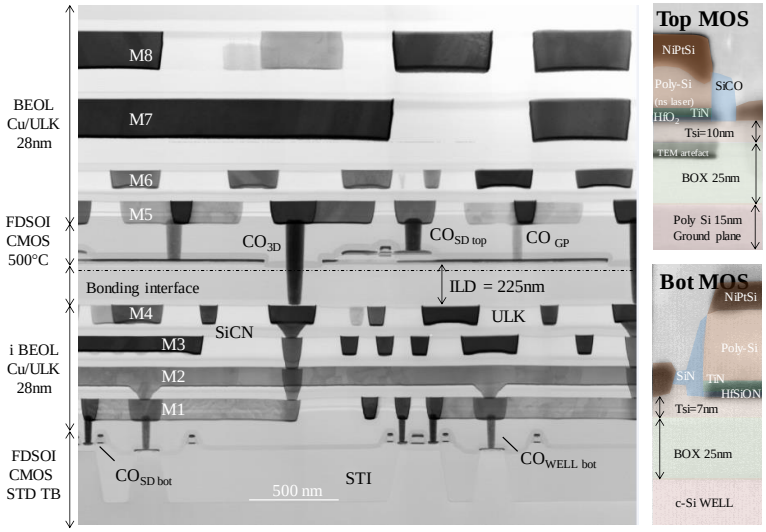
More testimonials here:
PhD Generation

More videos

Pioneering New Materials & Emerging Processes for Next-Generation Devices

REF: DCOS/LTA/DB-2026

Advanced SOI Technologies: Design, Integration & Electrical Characterization



Description

Join CEA-Leti to develop a technological module (localized ground plane) for various applications (EU FD-SOI, RF devices, ultra-miniaturized pixels, cryo-RF and quantum).

This PhD topic is challenging since you will design step by step a specific module and test it electrically. Our team will support you technically and scientifically to conduct this work. Some data are already available and waiting for your analysis.

During this PhD, you will have the opportunity to learn how a module/device is designed step by steps:

- From the idea (simulation, bibliography) 10%
- Material & Processes understanding (bonding, CMP) 30%
- Integration & cleanroom fabrication management 10%
- Characterization (physical & electrical: mobility, interface traps) 40%
- Valorization (presentations, article) 10%

This PhD offers a unique chance to be at the forefront of technological innovation and to make a significant impact in the field of advanced SOI. Join us and take the first step towards an exciting career in research and development!

Candidate Profile

With a background in microelectronics or nanotechnologies, you are curious about integration of new processes to build tomorrows transistors. You like to solve complex puzzles and enjoy collaborating with others to figure out innovative solutions.

 # Advanced technology
 # Cleanroom
 # Microelectronics
 # Design

Application & Societal Impact

More energy-efficient CMOS process

To go further

FDSOI technology

Your Supervisor Academic Profil

Team background

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor:
Daphnée Bosch

To apply, please contact:
Daphnee.bosch2@cea.fr

REF: DCOS/LDMC/GN-2026

Threshold Changeable Memory: Towards the Limits of Memory Scaling

Description

The explosion of Artificial Intelligence and Big Data demands memory solutions that are faster than Flash and denser than DRAM. Threshold Changeable Memory (or TCM) is one of the most promising candidates to fill this gap. A TCM device simplifies the memory cell by using a single material that acts both as the selector and the memory element. This enables ultimate device scaling and high density 3D stacked Crossbar arrays. However, the physical mechanisms governing its functionality and its stability in time and in temperature are still under debate.

This research project aims to bridge the gap between material properties and the device performance. You will be involved in the full development cycle of innovative TCM devices: material properties investigation of innovative chalcogenide alloys and transition metal oxides by combining different physico-chemical analyses; device integration and electrical characterization; modeling and optimization.

You will develop skills in material properties investigation techniques and analyses, nanodevice physics, electrical characterizations, device engineering within an interdisciplinary team of experts, working on a highly topical scientific and technological subject.

Candidate Profile

An excellent background is required in microelectronics, physics, materials science, you are curious and motivated to tackle scientific challenges. You have knowledge of semiconductor devices and characterization techniques, and you enjoy collaborative experimental work. Programming skills are a plus.

 # Memory
 # Microelectronics
 # TCM

Application & Societal Impact

In-Memory Computing for AI, Next-Gen Data Centers, Edge Computing & IoT

Energy Efficiency, Democratization of AI, Technological Sovereignty

To go further

"Rulebreakers' Revolutions: How SK hynix's SOM Paves the Way for Next-Gen Memory in the AI Era" SK Hynix 2025.

Our Technology

Key Challenge in this field

Your Supervisor Profile

To be inspired

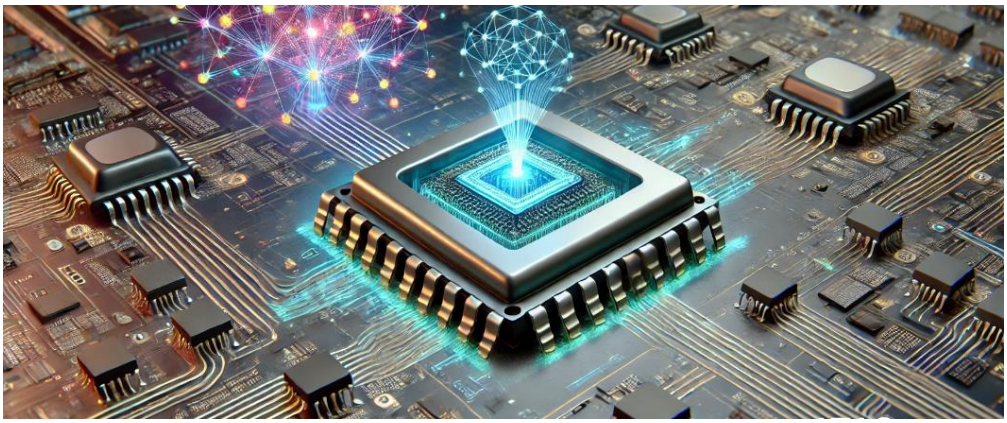
Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor:
G. Navarro

To apply, please contact:
gabriele.navarro@cea.fr

REF: DCOS/LDMC/LG-2026

Ultra Dense 3D Ferroelectric Memories



 # Semiconductor Oxide
 # Ferroelectrics
 # FeRAM bitcell
 # Advanced integration

Description

Join CEA-Leti for a very exciting experience working on both innovative materials (Semiconductor Oxide, Ferroelectric Hafnium Zirconium Oxide) and 3D advanced integration to develop the new generation of ferroelectric random access memories (FeRAM). This thesis offers the chance to work on a groundbreaking project, If you're curious, innovative, and eager for a challenge, you're welcome to join us!

The emergence of artificial intelligence, machine learning and Internet of things has driven the need for dense, ultra low power memories with high operation speed and non-volatile characteristics. Today, non-volatile ferroelectric memory technology, consisting of a Metal/Ferroelectric/Metal capacitor (1C) connected to the drain of a select transistor (1T), is very promising due to its high endurance, low writing voltage. The future of 1T1C ferroelectric memory requires innovation through ultra-low leakage and dense selector devices that can be integrated in the back-end of line (BEOL). Here, we propose to investigate 3D oxide semiconductor channel transistors as a new selector for the FeRAM bitcell.

Throughout the thesis, you will acquire a wide range of knowledge, covering microelectronic processes and integration, simulation, Oxide Semiconductor FET transistor fabrication and electrical characterization, and bitcell design. You will collaborate with multi-disciplinary teams to develop an in-depth understanding of ferroelectric memory devices as well as a wide range of potential applications. You will also be part of a memory device laboratory, working alongside a team of several permanent researchers (material, integration, electrical characterization and simulation) to support you in this research project.

Candidate Profile

With a background in microelectronics and a passion for technological research, you are curious, eager to learn, and possess strong communication skills. You have a keen interest in approaches that combine innovative material with emerging devices, particularly in the context of advanced memory integration.

Application & Societal Impact

- Ultra low-power embedded memories for AI and machine learning
- Energy-efficient storage

To go further

- N. Ramaswamy *et al.* "NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads", IEDM conference 2023. (Micron)
- S. Martin *et al.*, "Hf0.5Zr0.5O2 FeRAM scalability demonstration at 22nm FDSOI node for embedded applications", IEDM conference 2024. (CEA-Leti)

Our technology

Your Supervisor Academic Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor: L. Grenouillet

To apply, please contact:

laurent.grenouillet@cea.fr

REF: DCOS/LAPS/JB-2026

Development of Vertical GaN Power Transistors

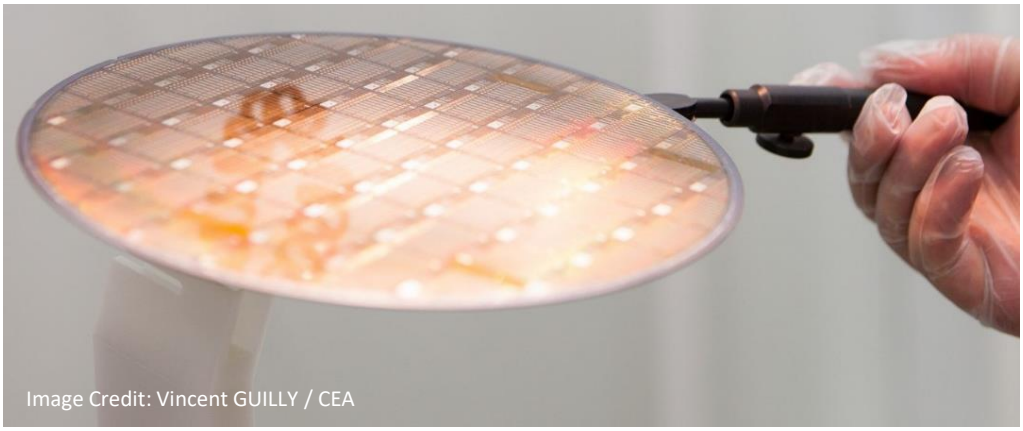


Image Credit: Vincent GUILLY / CEA

Description

Embark on an exciting technological journey with CEA-Leti! This Ph.D. offers a unique opportunity to enhance your skills in GaN power devices and develop cutting-edge architectures. You'll work alongside a multidisciplinary team specializing in material engineering, characterization, device simulation, and electrical measurements, with the potential to transition into a PhD program. If you're eager to innovate, expand your knowledge, and tackle state-of-the-art challenges, this position is a valuable addition to your career!

Vertical GaN power devices are highly promising for power applications beyond the kV range and are therefore extensively studied worldwide. Transistors with a 'trench MOSFET' architecture have been demonstrated in the state-of-the-art with very encouraging results. Their gate stack is a crucial element as it directly impacts on-state resistance, threshold voltage, and the control signal to be applied in a power converter. The proposed study in this thesis will focus on developing innovative gate stacks that can withstand high gate voltages while maintaining state-of-the-art threshold voltage and channel mobility with minimal gate dielectric trapping. The work will involve studying the impact of process parameters on electrical characteristics. Special attention will be given to optimizing the gate geometry through TCAD simulations to study how its shape impacts on-state and breakdown. Identified improvements will be integrated to the devices fabricated on our 200mm GaN power devices line. The Ph.D. will take place within the power devices lab in strong collaboration with the gate dielectric deposition team and our partner CNRS-LTM.

Candidate Profile

With a solid foundation in microelectronics devices and a high interest for technological research, you are eager to learn, have excellent communication skills and like to work as part of a team. You are particularly interested in methodologies that merge device physics with the electrical characterization of new device architectures for power electronics.

 # Gallium Nitride
 # Power Devices
 # Microelectronics
 # Gate Module

Application & Societal Impact

Propose energy-efficient power converters for reducing the carbon footprint of massive electrification

To go further

V. Ackermann *et al.*, https://doi.org/10.3390/mi16111193

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

The parter's team

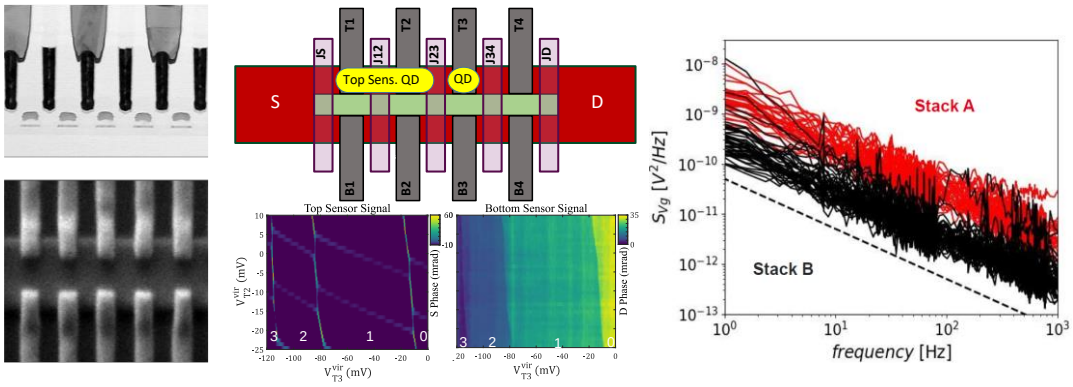
Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

PhD Advisors team:
Julien Buckley, Messaoud Bedjaoui, Aurélien Olivier, Bassem Salem

To apply, please contact:
julien.buckley@cea.fr

REF: DCOS/LDQ/HN-2026

Impact of Gate Materials on the Electrical Properties of Spin Qubits



 # QuantumComputing
 # Microelectronics

Description

Join the CEA-Leti R&D teams and be part of the revolution in quantum computing!

Spin qubits in semiconductors are a leading platform for quantum computing. Their fabrication benefits from decades of microelectronics industry advancements. However, while manufacturing processes are well-suited for traditional devices like transistors and memories, their effects on quantum devices operating under vastly different conditions (cryogenic temperatures, low current density) are still largely unknown. In particular, the quality of materials in close proximity to the active layers is of prime importance in order to achieve proper operability of spin qubit devices.

As PhD candidate, you will propose experiments focused on benchmarking materials quality and identifying sources of defects, with the help of CEA-Leti cleanroom experts. You will then characterize these experiments using various electrical testing techniques to extract key performance metrics for quantum devices. Your work will not only enhance our understanding of defects origins but also contribute to optimizing the fabrication processes for CEA-Leti's spin qubit devices.

You will receive expert guidance in the areas of fabrication, integration, and electrical characterization of semiconductor spin qubit devices. You will be encouraged to disseminate your research through publications, international conferences, and patents.

Candidate Profile

You possess a solid foundation in semiconductor physics, nanotechnology, and device characterization and fabrication. Your initiative and curiosity enable you to propose innovative solutions. You are also an excellent communicator.

Application & Societal Impact

- Significant increase of computing capability for healthcare, energy, transport, logistics, finance, defense, etc.

To go further

- B. Bertrand et. al., *Tunnel and capacitive coupling optimization in FDSOI spin-qubit devices*, IEEE IEDM, 2023

Our Technology

Key challenges

Characterizing Qubits

CEA-Leti manufacturing facilities

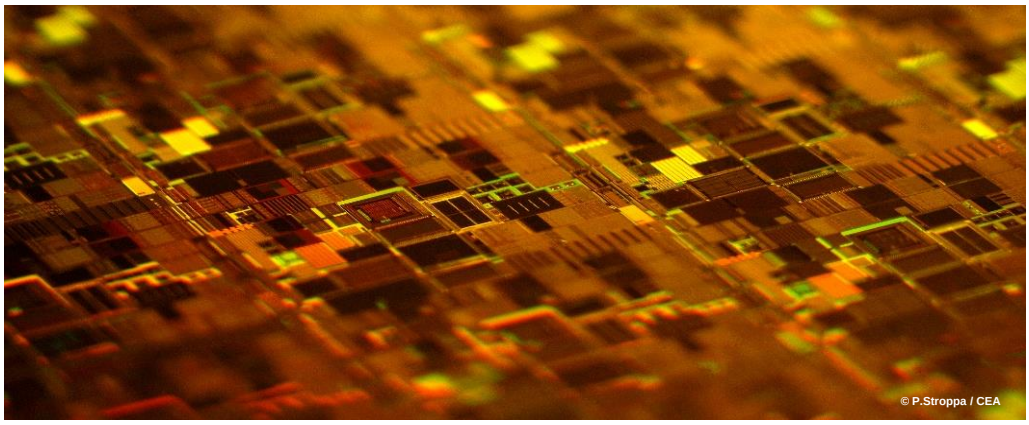
Starting date: Fall 2026
Duration: 36 months
Location: Grenoble, France
Supervisor: H. Niebojewski

To apply, please contact:

heimanu.niebojewski@cea.fr

REF: DCOS/LCRE/JC-2026B

All-Solid-State Microbatteries: Interface Stabilization and Degradation Mitigation



Description

Microbatteries and pseudocapacitors are emerging as key technologies for powering miniaturized systems such as wearable devices, autonomous IoT nodes, and implantable medical electronics. Unlike conventional batteries, these microscale energy storage devices face extreme constraints on size, thickness, and long-term reliability. Among the main challenges limiting their performance is the progressive increase of internal resistance during cycling and aging, largely driven by interface degradation.

This PhD project focuses on understanding and controlling interfacial phenomena in all-solid-state thin-film microbatteries based on $LiCoO_2$/LiPON/Li stacks. The work combines interface engineering using ultrathin ALD-deposited buffer layers with fundamental investigations of degradation mechanisms. The objective is to identify how nanoscale interlayers influence resistance evolution, stability, and lithium-metal behavior.

The research involves fabrication of thin-film stacks, electrochemical testing (CV, EIS, cycling), and advanced materials characterization (XRD, SEM, SIMS, confocal microscopy). The project also explores the use of alloying metals (Ag, Au, etc.) to stabilize lithium interfaces. Thanks to high-throughput wafer-level integration (>10,000 devices), statistically robust conclusions can be drawn.

The expected outcomes include an optimized microbattery architecture with exceptional cycling stability and a deeper physical understanding of interface degradation. Beyond microbatteries, the results will contribute to the broader field of solid-state batteries and materials screening methodologies.

Candidate Profile

You are a Master's student in Nanotechnologies, Materials Science, Physics, or a closely related discipline. You are interested in deepening your knowledge and expertise in energy storage, solid-state devices, and interface phenomena. Practical experience in thin-film deposition, microfabrication, electrochemical characterization, or materials analysis is a plus.

 # Interface-Engineering
#Solid-State Devices
 # Batteries

Application & Societal Impact

Enhancing Reliability of Miniaturized Energy Storage for Wearable and Medical Technologies

To go further

- Bates, J. B. et al., "Thin-film lithium and lithium-ion batteries ", Journal of Power Sources, 2000

Application Overview

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

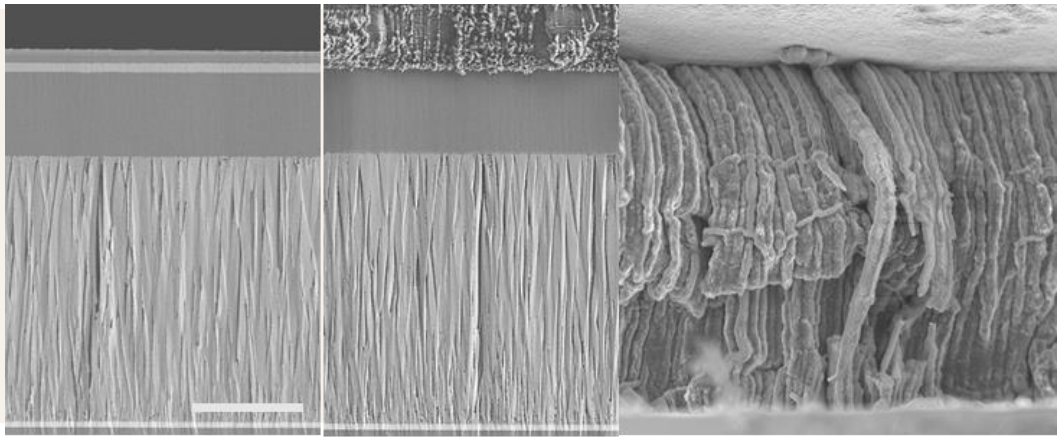
Supervisor: Jacopo CELÈ

To apply, please contact:

jacopo.cele@cea.fr

REF: DCOS/LCRE/JC-2026

Study of Mechanical Stress on All-Solid-State Microbatteries



 # Mechanics
 # µbatteries
 # Simulation
 # Electrochemistry
 # Characterization

Description

CEA-Leti provides integrated microstorage solutions, including solid state (or solid electrolyte) microbatteries. Solid-state micro-batteries are among the most promising microstorage technologies for applications in several fields such as the internet of things and implantable devices for medical use. Unlike conventional batteries, these microscale energy storage devices face extreme constraints on size and thickness that can affect long-term reliability. One of the key point for long term reliability is to understand the impact of mechanical stress during charge/discharge cycles of microbatteries.

The PhD student's work will begin with the development of mechanical test benches, the first of which will apply variable pressure to the surface of a microbattery during charge/discharge cycles. He/she will develop the pressure measurement equipment. Once the mechanical test bench is operational, other characterizations, such as measuring anode deformations, will be considered. In parallel with this experimental work, a mechanical model will be developed. This model will be progressively refined using the experimental results and new characterizations may be implemented in order to obtain the mechanical properties of the different materials used.

One of the practical outcome of this work will be to propose the integration of new “stressor layer” to improve the mechanical performance of microbatteries during cycling. The mechanical model will be useful to select the materials and geometry of this new stressor layer. Then it will be used to study new integrations allowing larger cathodes or to study the stacking of several batteries (dimensioning the interconnections). And finally the coupling between mechanics and electrochemistry will be studied.

Candidate Profile

You are a Master 2 student in Mechanical Engineering, Materials Science, or a closely related discipline. You are interested in understanding coupled physical phenomena (mechanics & electrochemistry) through both experimental and theoretical studies. Practical experience with mechanical characterization, finite element modelling or batteries is a plus.

Application & Societal Impact

Enhancing Reliability of Miniaturized Energy Storage for Wearable and Medical Technologies

To go further

D. Cao et al., Enhancing Lithium Stripping Efficiency in Anode-Free Solid-State Batteries through Self-Regulated Internal Pressure, Nano Letters, 2023

Application Overview

Our Technology

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor: Jean COLONNA

To apply, please contact:

Jean-philippe.colonna@cea.fr

REF: DCOS/LICA/RL-2026

MEMS Acoustic Transducers Integrating 3D Blades

Description

Are you looking for a PhD at the intersection of acoustics, microsystems, and innovation? This project may be for you. This PhD focuses on the design, fabrication, and experimental validation of an innovative MEMS microspeaker concept based on ultrasound demodulation. Conventional micro transducers face a major limitation: they require large planar surfaces to displace sufficient air at low frequencies, leading to increased device size and manufacturing cost. This project explores an alternative architecture using vertical blade structures, exploiting the third dimension together with ultrasound demodulation to improve electro acoustic efficiency while reducing device footprint.

Building on preliminary exploratory work, the objective of the PhD is to develop a complete MEMS loudspeaker demonstrator. The work will include physical modeling, multi-physics simulation, device design optimization, microfabrication process development, and experimental electro acoustic characterization. Particular attention will be given to identifying and overcoming the physical and technological limitations governing device performance.

The candidate will design and simulate the device architecture and contribute to the definition of the fabrication process in close interaction with microfabrication specialists. The PhD work will also include acoustic and electrical characterization of the fabricated devices in order to validate the proposed concepts and compare experimental results with modeling predictions. The PhD will take place in a multidisciplinary environment, providing access to expertise in acoustics, MEMS design, microfabrication processes, and electro acoustic measurement.

Candidate Profile

You hold an engineering degree or a Master's degree in acoustics, microsystems, physics, or a related field, with a solid background in electroacoustics, mechanics, or multi-physics modeling. You are curious, detail-oriented, and possess strong analytical and integrative skills. You excel at communicating complex ideas and enjoy tackling challenging design and simulation problems.

 # MEMS
 # Acoustics
 # Transducer

Application & Societal Impact

High-performance and reliable sensors/actuators

To go further

- MEMS loudspeakers review
- MEMS loudspeaker electrostatic
- MEMS loudspeaker piezoelectric
- Modeling electroacoustic MEMS
- Your Supervisor Academic Profil

Starting date: Fall 2026
Location: Grenoble, France

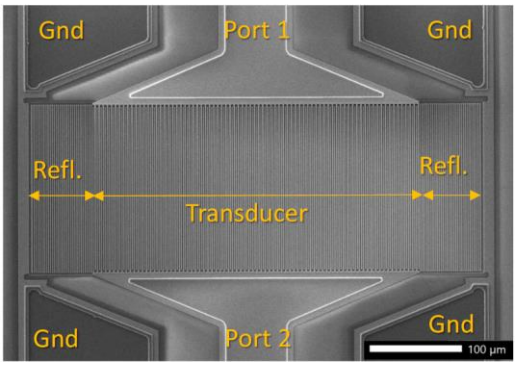
Supervisor: R. Liechti

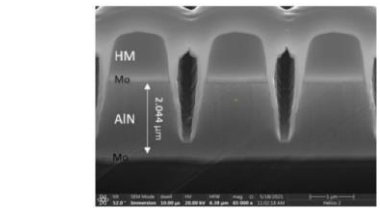
To apply, please contact:

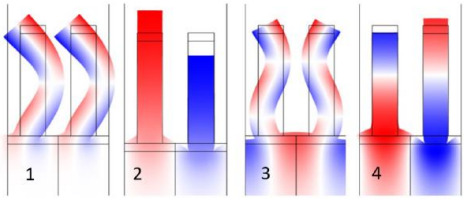
romain.liechti@cea.fr

REF: DCOS/LCRE/AR-2026

Topologically Isolated Mode Acoustic Resonators







Description

Timing is a key function in electronic circuits. Beyond on-chip signals synchronization, it also allows the synchronization of wireless data transmissions. Accurate time references require stable frequency sources, which also benefit to sensor applications. The gold standard for time or frequency generation is still quartz resonators, which are however bulky and difficult to miniaturize. Research is therefore still ongoing to provide high quality factor (> 10,000) resonators, ideally capable of operating at frequencies of several GHz. A key to reach such high quality factors is to confine strongly the mechanical vibration of micro-size structures in order to make them insensitive to external perturbations. Recently, the field of topological acoustics has demonstrated the capability to confine elastic waves in very small volumes concentrated near defects inserted in a periodic structure, and to provide extremely high quality factor resonances.

This PhD position focuses on exploiting topologically protected modes in piezoelectric microstructures to provide next generations of high quality factor resonators, which may be used in oscillators or even filter circuits. Leveraging the know-how of CEA Leti in the design and fabrication of such components, the PhD will be part of an international collaboration with well established academic laboratories (Politecnico di Milano, Imperial College FEMTO-ST Institute) and industrial partners.

The candidate will model and design structures supporting topologically protected modes, combinining finite element simulations with simplified numerical approaches which reduce computation times. He will follow the fabrication of demonstrators in collaboration with the process integration teams in the CEA Leti clean rooms, and carry on measurements of the proposed resonators.

Candidate Profile

We offer a unique internship opportunity for motivated students with a strong interest in RF devices, mechanical engineering and/or wave physics. Candidates with curiosity, rigor and a desire to tackle challenging problems are strongly encouraged to apply. Prior experience in numerical design (finite element models) will be appreciated. The ability to work in a multidisciplinary team will be essential to successfully carry out this research project.

 # Piezoelectrics
 # RF resonators
 # Acoustic waves

Application & Societal Impact

Energy efficient electronics

To go further

S. Barsoum, “High quality factor hybrid SAW/BAW resonators”, EFTF-IFCS 2022

J. M. De Ponti, “Localized topological states beyond Fano resonances via counter-propagating wave mode conversion in piezoelectric microelectromechanical devices”, Nature Communications 2024

Our Technology

Your Supervisor Academic Profile

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

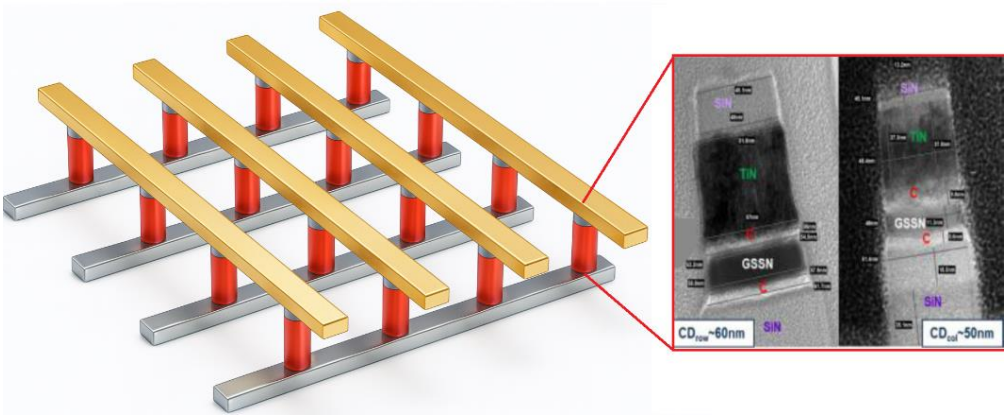
Supervisor:
Alexandre Reinhardt

To apply, please contact:
alexandre.reinhardt@cea.fr

Co-Optimize Technology & Circuit Design for Next-Generation Systems

REF: DCOS/LDMC/TH-2026

Selector-Only Memory (SOM/TCM) for Neuromorphic Circuit Design



 # Threshold Change Memory
 # Selector Only Memory
 # Memory Devices
 # In-Memory Computing
 # Neuromorphic

Application & Societal Impact

Smarter and energy-efficient artificial intelligence

Description

Join CEA-Leti to pioneer a new class of neuromorphic circuits based on Selector-Only Memory / Threshold-Controlled Memory (SOM/TCM) devices. This PhD builds on the revival of cross-point arrays—shifting from 1S1R (PCM/OxRAM + OTS) toward SOM/TCM stacks with lower operating voltages, simpler integration, and clear paths to 3D scaling for AI-era density and bandwidth.

Modern AI models require memory systems that are simultaneously dense, fast, and frugal. Conventional current-mode reads burn power and risk disturbing device states. In this project, you will (i) explore robust biasing and forming/programming strategies for OTS-based TCM cells, (ii) design and validate a capacitive read that charges a sensing node cutting read energy and minimizing read-disturb—and (iii) exploit the devices' transient/oscillatory regimes to implement neuromorphic primitives (neurons/synapses) directly in memory

Your work will span device-to-algorithm co-design: Verilog-A compact modeling and SPICE-level circuit design prototype SOM/TCM test chips and electrical characterization, and system-level evaluation of neural networks performances under realistic device constraints. You will work within Leti's fabrication and test platforms and in close collaboration with IM2NP; the thesis is supervised by Prof. Jean-Michel Portal.

If advancing ultra-low-power neuromorphic computing excites you, this PhD offers end-to-end, hands-on experience—from nanodevices to neuromorphic systems—at the intersection of AI and nanotechnology.

Candidate Profile

With a background in microelectronics, you are a problem solver with strong adaptability and communication skills. You are curious and you like experimental team work. You have a keen interest in both emerging electronic devices and artificial neural networks applied to next-generation AI systems.

To go further

S. Ban et al., "Achieving Outstanding Endurance (>10^7) in Large-Array Two-Deck 16 Nm SOM Through Process, Structure, and Design Strategies for Emerging SCM Applications," VLSI'25

Y. Seo et al., "Multi-Stack InTe Selector-Only Memory (SOM) Achieving Ultra-Low Power Operation (10 μA) and Excellent Endurance (~ 10^{10} cycles)," VLSi'25

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisors: T. Hirtzlin, J. Minguet-Lopez, Jean Michel Portal

tifenn.hirtzlin@cea.fr
joel.minguetlopez@cea.fr

REF: DCOS/LTA/MC-2026

SiGe HBT Low Noise Amplifiers for Cryogenic Applications

Description

Join CEA-Leti to contribute to the development of electronics operating at extremely low temperatures (down to 4 K and below), with applications such as quantum computing, radio astronomy, or particle detectors,. This PhD position offers the opportunity to work on advancing BiCMOS technology for emerging fields.

The global race to build a quantum computer is heating up! These cutting-edge systems operate at temperatures below 4 K to preserve the delicate quantum states essential for computation. To achieve efficient control and detection, conventional electronic circuits must perform reliably at cryogenic temperatures, in close proximity to the quantum processor, thereby reducing wiring complexity and boosting performance. Beyond quantum computing, other domains—such as space exploration, high-performance computing, or high-energy physics—also require CMOS transistors capable of operating below 100 K.

During this PhD, you will perform radiofrequency (RF) electrical characterization and modeling of Silicon-Germanium Heterojunction Bipolar Transistors in cryogenic environment, contributing to a deeper understanding of their behavior and optimizing their potential for extreme-condition applications. The objectives are twofold:

1. RF Electrical Characterization and Modeling: Conduct RF electrical measurements of SiGe HBTs at cryogenic temperatures. Develop accurate models to describe their behavior in cryogenic environments.
2. Optimization of Low-Noise Amplifiers (LNAs): Study the low-temperature behavior of individual passive and active devices composing an LNA. Optimize the design of low-noise amplifiers (LNAs) for cryogenic applications.

Candidate Profile

We are looking for a motivated student with a background in microelectronics, device physics, or RF electronics, who enjoys experimental work and is eager to explore new research domains beyond conventional electronics. Curiosity, teamwork, and the ability to thrive in an international, multidisciplinary environment are essential. If you're passionate about pushing the boundaries of electronic technology and making a significant impact on future innovations, this PhD is your opportunity!

 # Cryoelectronics
 # Electrical characterization
 # RF circuits and devices

Application & Societal Impact

Quantum computing
Spatial applications

To go further

Q. Berlingard, Ph.D thesis, UGA, 2024, HAL Id: tel-05029005

J. D. Cressler, “The SiGe HBT at Cryogenic Temperatures,” 2023

Doi:10.1109/BCICTS54660.2023.10310965

STMicroelectronics B55x technology

CryoCMOS for Quantum Computing

Quantum Computing @ CEA

The ARCTIC project

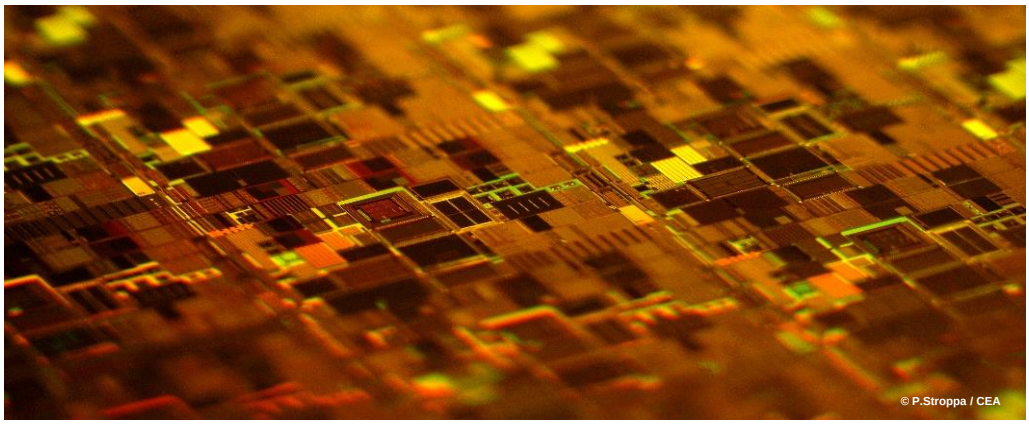
Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor:
J. Lugo & M. Cassé

To apply, please contact:
mikael.casse@cea.fr

REF: DCOS/LCRE/JC-2026A

Interface, Switching Dynamics and Circuit-Level Modeling of Anti-Ferroelectric HfO_2 Capacitors



Description

In fully integrated power converters, capacitors often dominate the chip or package footprint, limiting further miniaturization and power-density improvements. Among emerging solutions, capacitors based on ferroelectric (FE) and antiferroelectric (AFE) materials offer promising pathways toward significantly higher performance compared with conventional linear dielectrics.

This PhD project focuses on doped HfO_2-based thin-film capacitors, a material platform that uniquely combines CMOS compatibility with ferroelectric or antiferroelectric switching behavior.

While these functional oxides enable enhanced energy-storage capabilities, their strongly nonlinear and history-dependent response—characterized by hysteresis, minor loops, and relaxation phenomena—poses major challenges for circuit design and simulation.

This research project combines experimental, physical, and modeling approaches, including: fabrication and electrical characterization of thin-film MIM capacitors; systematic analysis of polarization-switching and relaxation dynamics; the development of circuit-compatible compact models. Multiphysics and numerical modeling tools will support the interpretation of experimental results and guide model development.

The expected outcomes include a validated modeling framework for FE/AFE capacitors and design-relevant insights into their use in DC–DC converters. Beyond capacitor technology, the results will contribute to the broader understanding of functional oxides in integrated electronic systems.

Candidate Profile

You are a Master's student in Nanotechnologies, Materials Science, Physics, Electrical Engineering, or a closely related discipline. You are interested in deepening your knowledge and expertise in functional materials, energy-storage devices, and advanced electronic components. Practical experience in thin-film technologies, electrical characterization, device physics, or numerical modeling (Python, COMSOL, etc.) is a strong plus.

 # Supercapacitors
 # Anti-Ferroeletricity
#Solid-State Devices

Application & Societal Impact

Advancing High-Density Integrated Capacitors for Miniaturized Power Electronics

To go further

- S.-H- Yi et al., Ultra-high energy storage density and scale-up of antiferroelectric TiO2/ZrO2/TiO2 stacks for supercapacitors, J. Mater. Chem. A 2021

Application Overview

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

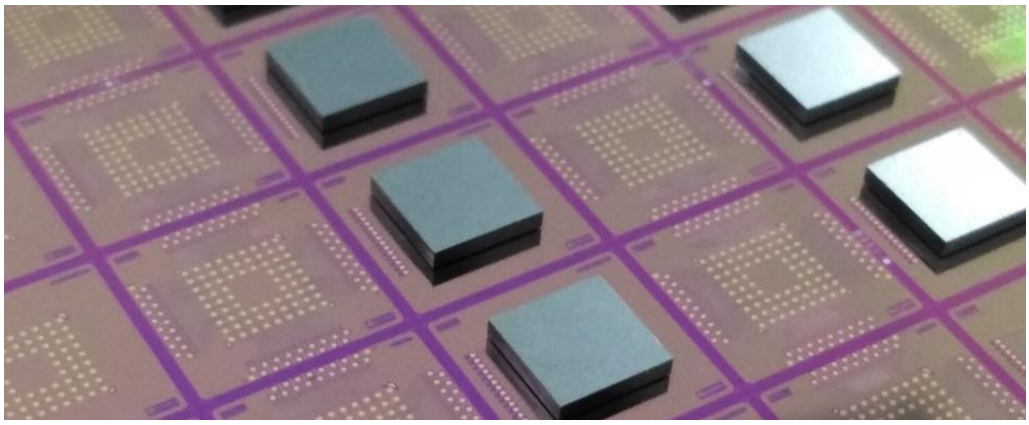
Supervisor: Jacopo CELÈ

To apply, please contact:

jacopo.cele@cea.fr

REF: DCOS/LTI3D/CT-2026

3D Interconnects for Quantum Processor



Description

To increase the performance of quantum computers, three-dimensional (3D) integration is now the key! Using technologies such as flip-chip bonding, multi-layer wiring or even through-silicon vias (TSV), 3D integration offers solutions to increase the number of qubits on a processor, reduce signal loss and cross-talk and even improve thermal management. All of these aspects are essential to continue scaling qubits to achieve fault-tolerant quantum computing.

Our team is developing 3D interconnect technologies (e.g. superconducting microbumps and TSV) for the next generation of quantum processors. This thesis will focus on characterizing such interconnects through electrical and radiofrequency measurements at low temperatures to gain knowledge on how they may impact quantum device properties when integrated nearby.

This position will bring you at the boundary between material, technological and physical challenges of quantum systems. You will work in a collaborative environment with teams from CEA-LETI and CEA-IRIG. As a PhD candidate, you will participate to the layout of a new mask set aiming to investigate new designs co-integrating 3D bricks and quantum devices. You will contribute to the fabrication of the wafers and the 3D assemblies using 200 mm Si wafer technologies. You will then carry on the low temperature measurements of the integrated structures and the data analysis.

Candidate Profile

You have a master or engineering degree with a specialization in quantum physics, microelectronics or nanotechnology and are highly motivated to contribute to cutting-edge research. Any experience in cleanroom processes, low temperature electrical characterizations and/or layout is a plus. Strong python programming knowledge is a clear asset.

 # Quantum Computing
 # 3D integration
 # Spin qubits
 # Superconductors

Application & Societal Impact

Large-scale quantum computing

To go further

C. Thomas *et al*., Materials for Quantum Technology, 5, 016001, (2025)

- Our Qubit Technology
- Our approach for Qubit Communication
- Our 3D integration expertise
- Your Supervisor Academic Profil
- Strong collaboration with physicists

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France
Supervisors: Candice Thomas and Simon Zihlmann
PhD director: Xavier Jehl

To apply, please contact:
candice.thomas@cea.fr

REF: DCOS/GP-2026

Innovating Power Management From Leti's Emerging Devices

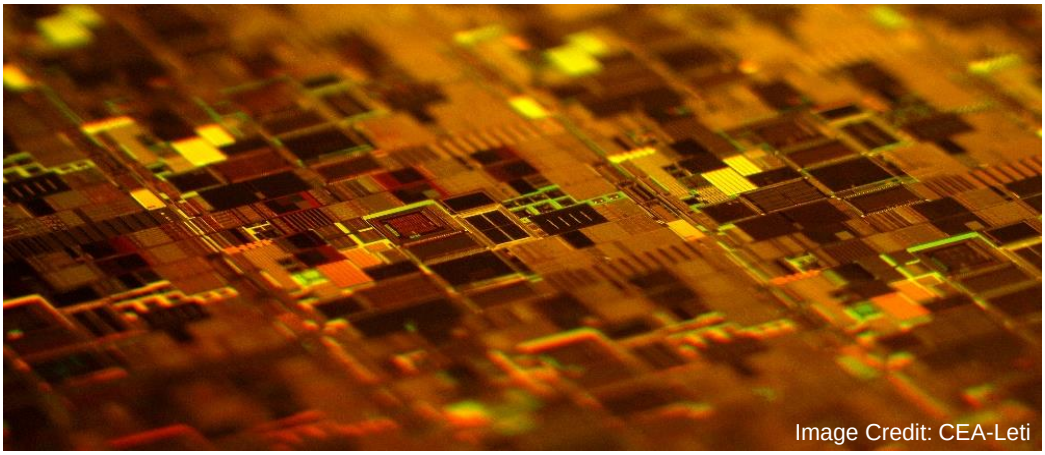


Image Credit: CEA-Leti

Description

The rapid growth of large AI models is driving demand for power-intensive, high-performance computing infrastructures deployed in massive data centers. Future facilities are projected to operate at gigawatt scale, creating major challenges for next-generation power delivery architectures. Recent advances emphasize the need for disruptive approaches, notably vertical power delivery, to satisfy the extreme requirements of AI processors.

In this PhD, you will contribute to defining next-generation power delivery technology stacks capable of sustaining unprecedented power densities using emerging devices fabricated in Leti's cleanroom. Building on our unique portfolio - from vertical GaN power transistors and high-density silicon capacitors to state-of-the-art hybrid bonding - you will assess the most promising technology combinations.

Using preliminary data from novel devices and system-level constraints, you will explore several scenarios to deliver first-order evaluations of performance potential and limits. These insights will steer the PhD toward a targeted implementation integrating advanced devices, IC design, and packaging.

You will collaborate with experts spanning system architecture to semiconductor devices, consolidating their inputs into a structured framework for innovative power delivery technology stacking.

Candidate Profile

You have a background in microelectronics and enjoy tackling complex problems with adaptability and strong communication skills. Curious and collaborative, you have a interest in process technologies, devices, IC design, power electronics.

 # Power Management
 # DTCO
 # IC design

Application & Societal Impact

Crossing Boundaries: Device-to-System Innovations for break Power wall

To go further

L. Su, "Innovation For the Next Decade of Compute Efficiency.", ISSCC, 2023.

G. Pillonnet, "Analytical Benchmarking of Direct Hybrid Switched-Capacitor DC-DC Converters." IEEE Open Journal of Power Electronics, 2024.

Application Overview

Our Technology

What is PMIC ?

Your Supervisor Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor: Gaël Pillonnet

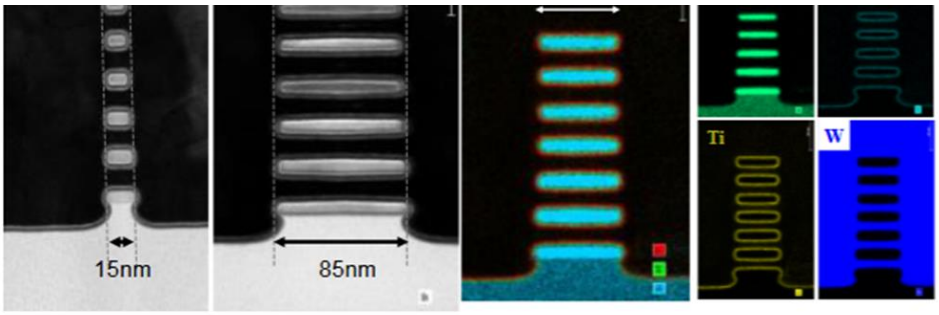
To apply, please contact:

gael.pillonnet@cea.fr

Characterization & Modeling for Deeper understanding of Emerging Devices

REF: DCOS/LSM/SJ-2026

Strain Engineering for CFETs: Modelling and Characterization



Description

A few years ago, CEA-Leti demonstrated the fabrication of new gate-all-around (GAA) nanosheet devices as an alternative to FinFET technology, in order to target high-performance (HPC) applications used in smartphones or laptops. In order to increase the components density, a CFET architecture is now under development. CFETs is basically composed of 2 GAA, n- and pMOS devices stacked on top of each other. The goal of this PhD is to develop our skills in strain engineering for CFET devices. Strain engineering consists in introducing stress into the channels of CMOS devices to boost their electrical performances. The student will use commercial codes dedicated to FEA (Ansys, Comsol Multiphysics) or specific to process flow modeling (Sentaurus). Experimental work will be done with our colleagues of the Nanofabrication Platform in order to validate the modeling work, in particular by the use of a very powerful technique, TEM-PED, aimed at monitoring strain at a very small spatial resolution of a few nanometers.

This PhD will give an unique opportunity to acquire a large scope of skills in the field of advanced microelectronics.

Candidate Profile

You are have a M2-level degree in the field of physics or materials science. Passionate by scientific and technological research, you are interested in numerical simulation and experimental work. You have knowledge in solid-state physics, numerical simulation methods, and have some understanding of or interest in semiconductors technology.

 # Advanced CMOS
 # CFETS
 # Simulation
 # Characterization

Application & Societal Impact

New technology development

For power reduction

To go further

S. Barraud et al., “7-Levels-Stacked Nanosheet GAA Transistors for High Performance Computing

Application Overview

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

The simulation code

About TEM-PED

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

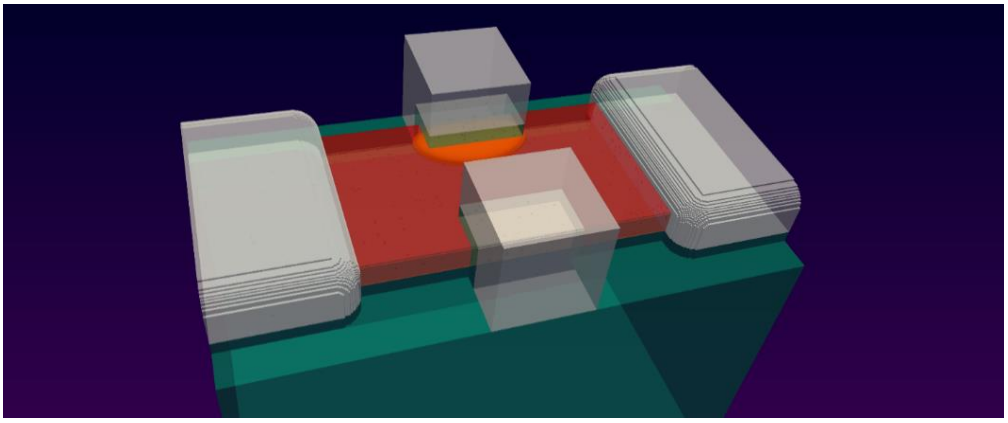
Supervisor: Sylvie Jarjayes

To apply, please contact:

sylvie.jarjayes@cea.fr

REF: DCOS/LSM/BM-2026

Multi-scale Modelling of Charge Noise in Spin Qubit Devices



Description

Thanks to strong collaborations between teams from several research institutes and the cleanroom facilities at CEA-Leti, Grenoble has been a pioneer in the development of spin qubit devices as a platform for quantum computing. The lifetime of these spin qubits is highly sensitive to fluctuations in the qubit's electrical environment, known as charge noise. Charge noise in spin qubit devices potentially originates from trapping/detrapping events within the amorphous and defective materials (e.g., SiO_2, Si_3N_4). This project aims to better understand the origin of this noise through numerical simulations, and guide the development of quantum devices towards lower noise levels and higher quality qubits.

The goal of this position is to improve the understanding of noise in spin qubit devices through multi-scale simulations going from the atomistic to the device level. The PhD candidate will use codes developed at CEA for the numerical modeling of spin qubits and will leverage supercomputing facilities to perform the simulations. Depending on the candidate's profile and interests, code development may be considered. The work will also involve collaborations with experimentalists to validate simulation methods and to aid in the interpretation of experimental results.

Candidate Profile

You are currently pursuing an M2-level degree in the field of theoretical physics, chemistry or materials science. You are passionate about scientific and technological research and are interested in numerical simulation and quantum computation. You have knowledge in solid-state physics, numerical simulation methods, and have some understanding or interest in spin qubits.

 # Quantum Computing
 # Spin Qubits
 # Simulation
 # Charge noise

Application & Societal Impact

- New computational paradigm

To go further

- B. Martinez: Phys. Rev. Applied 17, 024022 (2022).

Application Overview

Our Technology

Key Challenge in this field

Your Supervisor Academic Profil

The simulation code

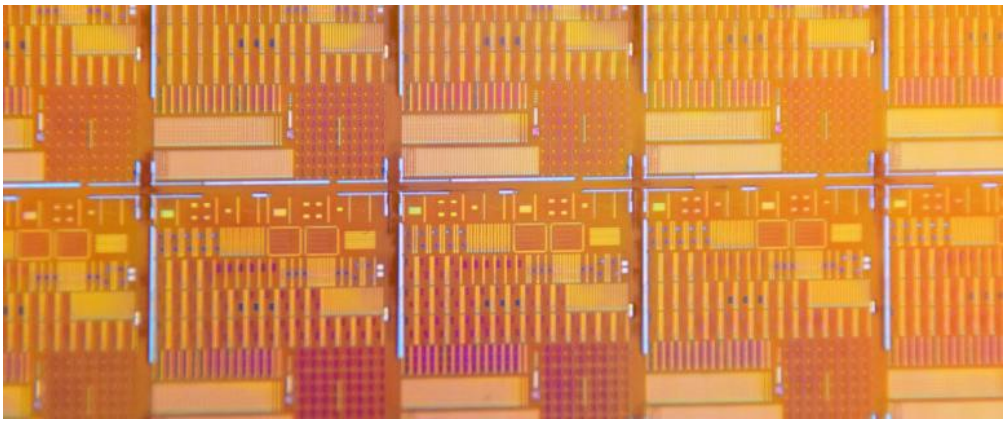
Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France
Supervisor: Biel Martinez i Diaz

To apply, please contact:

biel.martinezidiaz@cea.fr

REF: DCOS/LCEF/JR-2026

High-Endurance Chalcogenide Memories for Next-Generation AI



 # Memory Devices
 # Microelectronics
 # In-Memory Computing

Description

This PhD offers a unique opportunity for motivated students to contribute to cutting-edge research in advanced Chalcogenide-based memory technologies. The project focuses on Phase-Change Memory (PCM) and Threshold Change Memory (TCM), two promising candidates to bridge the gap between memory and storage in Artificial Intelligence applications where speed and endurance are critical.

PCM has already reached high maturity in both standalone and embedded markets. Despite the theoretical promise of virtually infinite endurance, device cycling remains limited due to the progressive evolution of the chalcogenide material. TCM, on the other hand, is a more recent concept. While less mature and with fewer studies available, it shares the same material systems as PCM and exhibits similar challenges related to material evolution and endurance.

The aim of this work is to investigate the physical origins of cycling degradation in PCM and TCM devices and to propose innovative strategies to overcome these limitations. The student will conduct advanced electrical characterization of state-of-the-art devices, complemented by physico-chemical analyses such as TEM to analyze degradation phenomena. A further objective will be the exploration of new programming protocols designed to mitigate or even suppress endurance issues.

The PhD provides hands-on access to advanced experimental platforms and the opportunity to work closely with multidisciplinary teams, including specialists in device physics and materials science.

Candidate Profile

With a background in microelectronics, physics, or materials science, you are curious and motivated to tackle scientific challenges. You have knowledge of semiconductor devices and characterization techniques, and you enjoy collaborative experimental work. Programming skills in Python or R are a plus.

Application & Societal Impact

Smarter and energy-efficient artificial intelligence

To go further

- ”Managed-Retention Memory: A New Class of Memory for the AI Era” S.Legtchenko

Our Technology

Key Challenge in this field

Your Supervisor Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

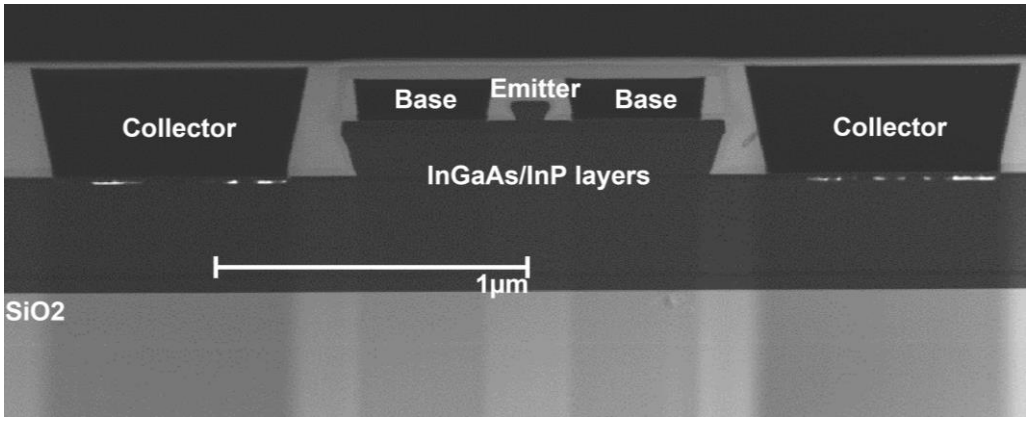
Supervisors: J. Rottner & G. Navarro

To apply, please contact:

jean.rottner@cea.fr

REF: DCOS/LTA/AD-2026

Electrical Characterization and optimization of III-V HBT on Si for 6G and datacom applications



 # RF transistors
 # Microelectronics
 # 6G – sub-THz
 # SPICE modeling

Description

Join CEA LETI for an exciting PhD program where you will work on high-speed III-V transistors designed for integration with CMOS circuits, to shape the future of 6G communications and optical datacoms for AI datacenters.

As digital content demand surges, 6G systems face major challenges, particularly in developing power amplifiers for Sub-THz frequencies. These frequencies promise ultra-high data rates but push the limits of current silicon technology. In AI datacenters, optical communication between GPUs is a must to reduce the total energy usage, compared to classical wiring. The highest speed devices are then needed in photodetectors & lasers' electrical drivers. InP-based Heterojunction Bipolar Transistors (HBTs) on large silicon substrates offer a promising solution, combining high-speed performance with minimal system losses. This technology comes with the challenges of integrating III-V layers with CMOS-compatible processes while allowing promising new device architectures, for both electrical parasitics reduction and self-heating management.

This PhD program aims to guide Leti's III-V HBT on Si developments to optimize the device architecture and increase the RF performance.

In this program you will :

1. Perform electrical characterization of various device geometries and technological splits through DC and RF measurements such as IV, thermal analysis, S-parameters and possibly Load-Pull.
2. Simulate key parasitics and new device architectures to understand device limitations
3. Collaborate closely with process engineers to link electrical results with fabrication choices and guide device optimization.

Candidate Profile

With a background in radiofrequency and/or microelectronics, you are a problem solver with strong adaptability and communication skills. You are autonomous and you like experimental work. You have a keen interest in both emerging electronic devices and 6G telecommunications.

Application & Societal Impact

Smarter and energy-efficient devices for 6G telecom,

Reduction of AI datacenter energy consumption (optical datacom)

To go further

- Intel Corporation, "Indium-Phosphide Transistors: A Review of Current State and Suitability for Commercial > 100-GHz Wireless Communication Systems", IEEE Microwave Magazine, v25 Issue 10, 2024
- A. M. Arabhavi et al., "InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With fMAX = 1.2 THz," in IEEE Transactions on Electron Devices, vol. 69, no. 4, pp. 2122-2129, April 2022

PEPR-electronique.fr/T-REX 6G

https://www.move2thz.eu/

Your Supervisor Academic Profile

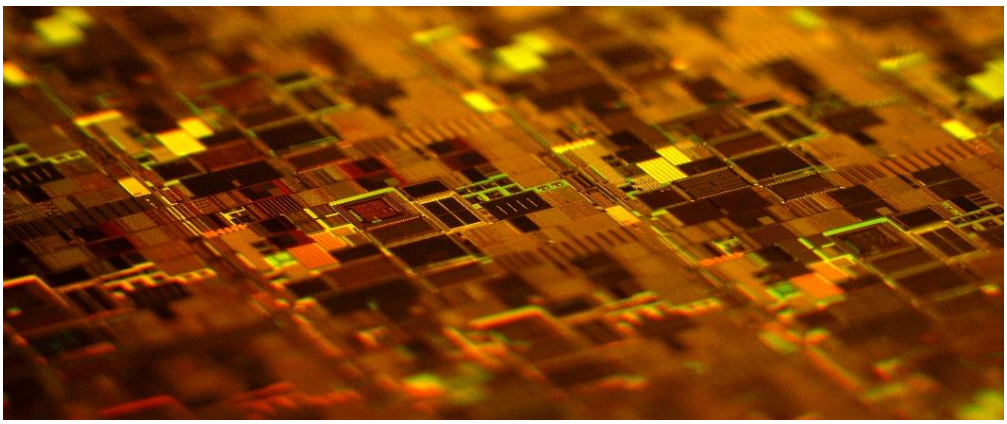
Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor: A. Divay

To apply, please contact:
alexis.divay@cea.fr

REF: DCOS/LCEF/RL-2026

Reliability and Dynamic Properties of GaN HEMT



Description

The rapid expansion of AI and cloud computing has placed unprecedented demands on data center infrastructure, where energy efficiency is now a defining constraint. Despite their potential, many power systems still rely on silicon-based devices, which suffer from inherent efficiency limitations that result in significant energy losses. GaN HEMTs, with their superior electron mobility and high breakdown voltage, represent a compelling alternative, capable of achieving far higher efficiencies in power conversion. However, their broader adoption is constrained by reliability challenges, particularly those arising from charge trapping mechanisms that degrade device performance over time.

In this PhD project, you will delve into the fundamental dynamics of charge carriers in GaN HEMTs, focusing on the physical origins of on-resistance and threshold voltage drifts—key indicators of device instability. By systematically analyzing the electrical behavior of these transistors under various operating conditions, you will uncover the mechanisms behind their degradation and identify pathways to enhance their robustness. Your findings will directly inform the optimization of device architectures, enabling the development of more efficient and reliable power electronics that can meet the demands of modern data centers and beyond.

You will be part of a multidisciplinary research team at CEA-Leti, collaborating with experts in semiconductor material engineering, device simulation, and electrical characterization. This environment will provide you with a comprehensive skill set, spanning process engineering, advanced electrical testing, and TCAD simulations, This position will not only expand your expertise but also position you at the forefront of a field with global impact. By contributing to the advancement of GaN HEMTs, you will play a key role in shaping the future of power electronics—where innovation directly translates into sustainable technological solutions.

Candidate Profile

With a solid foundation in physics of semiconductor devices and a fervor for technological research, you are eager to learn, and have excellent communication skills. You are particularly interested in methodologies that merge device physics with the electrical characterization of new device architectures for power electronics.

 # Microelectronics
 # Power Devices
 # Electrical characterization

Application & Societal Impact

Minimizing energy dissipation in power converters for data centers

To go further

- https://theses.hal.science/tel-04634491v1
- https://cea.hal.science/cea-03870230/document
- C. Masante et al., "Improved Normally-Off 1200 V GaN-on-Si MOS-HEMT with Novel AlGaN Back Barrier," 2025

Our Technology

The Great Debate at APEC 2025: GaN vs. SiC

GaN Power HEMT

Your Supervisor Academic Profil

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

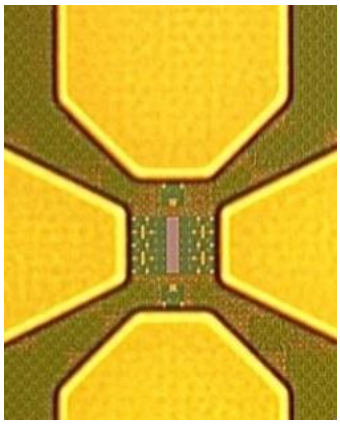
Supervisor: Romain Laviéville

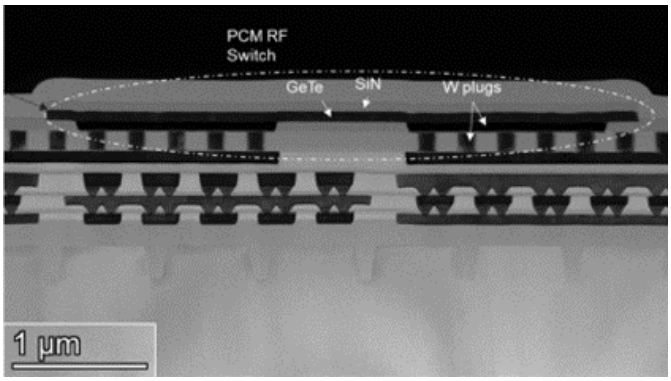
To apply, please contact:

romain.lavieville@cea.fr

REF: DCOS/LCEF/SM-2026

Study of Failure Modes and Mechanisms in RF Switches Based on Phase-Change Materials





Description

Are you seeking a multifaceted PhD subject? This subject is ideal for you, as it sits at the intersection of materials science, microelectronics, and reliability engineering.

You will focus on investigating the reliability and performance of RF switches utilizing phase-change materials (PCM). Beginning with a comprehensive bibliographic analysis and a review of internally available data, you will analyze various failure modes observed in these switches under different operational conditions, including endurance, state stability, and power handling. Key tasks will involve conducting experimental tests, performing detailed failure analyses and executing multiphysics numerical simulations to define one or more degradation scenarios. The ultimate goal is to identify critical failure mechanisms and modes, and to propose design, process, and integration improvements to enhance the reliability (= lifetime) of PCM RF switches.

This interdisciplinary research will span fields such as materials science, microelectronic manufacturing processes, electrical testing, reliability studies, including failure analyses and numerical simulations. You will benefit from the support of laboratories specializing in the manufacturing and integration processes of PCM RF switches, as well as electrical characterization and reliability. Collaboration with the nano-characterization platform (PFNC) will further enrich the resources available for this project.

You will document your findings in detailed reports and present your results to the research team and at international conferences. This opportunity offers hands-on experience in cutting-edge materials science and RF technology.

Candidate Profile

Trained in materials science, with a preferred background in micro/nano technology manufacturing processes, you are curious, detail-oriented, and possess strong analytical and synthetic skills. You have excellent communication abilities and a passion for hands-on experimental work.

 # Materials
 # Phase Change Memory (PCM)
 # Reliability
 # Failure analysis

Application & Societal Impact

High-performance and reliable PCM RF switches

To go further

- Introduction to PCM RF switches
- Introduction to Reliability
- Our last achievement
- One PhD thesis @LETI
- Your Supervisor Academic Profile

Starting date: Fall 2026
Duration: 3 years
Location: Grenoble, France

Supervisor: Stéphane Moreau

To apply, please contact:
stephane-nico.moreau@cea.fr

Discover our unique Technological Environment

CEA-Leti's Cleanrooms Platform

Manufacturing innovative devices for the industry

Main Activities

- More Moore microelectronics, Beyond CMOS & More than Moore
- Substrates and substrate engineering, including SOI and FD-SOI
- Power components
- MEMS and NEMS
- Non-volatile memory
- Imagers and displays
- Silicon photonics
- 3D integration

Key figures

- 14,000 m² space
- 600 research engineers
- 50 new patents a year

CEA-Leti's teams support the innovation needs of industrial partners across all or some stages of development, using bilateral contracts. Each collaboration is subject to an intellectual property agreement establishing the confidentiality of all work.
The platform works with more than fifty industrial partners: microelectronics stakeholders, fabless companies and equipment manufacturers, industrial users (telecoms, photonics, automobile equipment manufacturers, etc.)

With a world class microelectronic equipment pool, CEA-Leti's cleanrooms help develop procedures involved in manufacturing innovative components and electronic circuits compatible with the industry's high-volume requirements. CEA-Leti's cleanrooms are ISO 9001 certified and are in operation 24h/7.

More than 600 CEA-Leti experts in microelectronic processes (deposition, photolithography, etching, planarization, bonding, etc.), equipment, and materials are developing technologies and components for future products in collaboration with many industrial partners (lab-to-fab model) :

- resilient, competitive manufacturing processes with an optimized number of stages and environmental impact;
- customized, ready-to-use multistage modules for smooth transfers to our industrial partners' production machines;
- state-of-the-art prototypes in terms of miniaturization, energy efficiency, speed, frequency, and performance.

The platform relies on a pool of nano-characterization equipment that is unique in Europe, including electron microscopy, X-ray diffraction, magnetic resonance, ion beam processes.

Photo credit: A.AUBERT/CEA

Nanocharacterization Platform

Characterization of advanced materials and components supporting disruptive innovation

Main Activities

- Magnetic resonance
- Scanning probe microscopy
- Ion beam analysis
- Surface analysis
- Optics & X-rays analysis
- Electron microscopy
- Sample preparation
- Digital data processing

Key figures

- 3,600 m² of equipment
- 100 research engineers
- 90 publications a year
- €35M of cumulated investments

CEA-Leti's teams support the innovation needs of industrial partners throughout all development stages via bilateral contracts and shared laboratories. The platform works with more than a dozen partners, such as: SERMA Technologies, Physical Electronics (ULVAC-PHI) and Attolight.

The nano-characterization platform offers an access to over 100 researchers that operate state-of-the-art equipment and analyse properties of innovative materials and components.

With more than 50 world-class equipment, researchers supports companies of all sizes, from startups to major groups. They provide in-depth analysis, investigating new materials and components properties—morphological, physical, chemical, and electrical behaviors. They also collaborate with nanocharacterization tools suppliers to improve their equipment performance.

To be more specific, our researchers characterize advanced materials, complex stacks, new devices and manufacturing processes using customized analysis and characterization protocols. They also leverage large scale infrastructures, partnering with ESRF and ILL, as well as other key academic partners.

They also provide results and interpretations, such as atomic-scale 2D mapping, multi-scale 3D reconstructions, multi-scale composition analysis (from µm down to sub-nm), crystallographic structures, optical properties, and surface compositions.

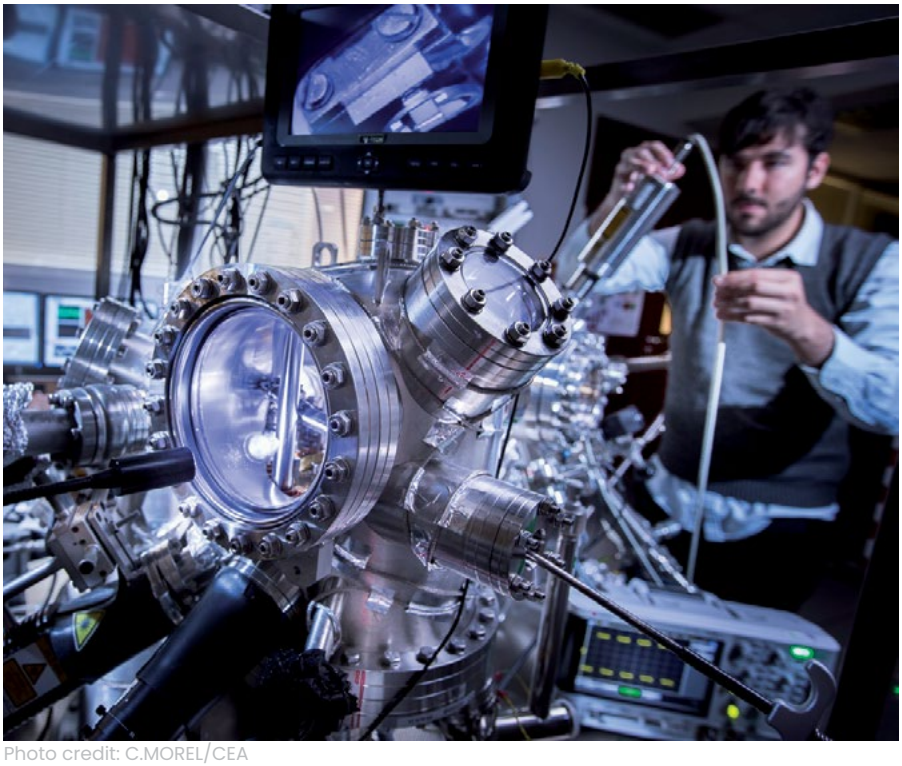


Photo credit: C.MOREL/CEA

Power Electronics Platform

Achieving optimal performance and accelerating the adoption of GaN and SiC technologies

Main Activities

- New GaN & SiC generations
- Prototyping

Key figures

- 14,000 m² space
- 100 research engineers
- 100+ patents in our portfolio
- 20 industrial partners

CEA-Leti's teams support the needs of its industrial partners (major groups, small and medium-sized companies, and startups) across all or some stages of development, using bilateral contractors or shared laboratories. The platform hosts about twenty industrial partners from the microelectronics sector or specialized in power components. Amongst them are Renault, Schneider Electric, Soitec, STMicroelectronics, Valeo, etc. Partnerships have been established with several of these industrial market leaders.

The platform is developing innovative substrates, components, and architectures devoted to power conversion, from the design stage to a functional demonstrator. With pre-industrial equipment, it offers customized support to industrial partners.

The platform is open to the transport industry (two-wheelers, automobiles, rail transport), data centers, photovoltaics, etc. R&D projects have three objectives:

- improving conversion and energy efficiencies in systems;
- making innovative components and systems more reliable, or even qualifying them for targeted applications, aiming for performance that is at least equivalent to that of marketplace silicon solutions;
- reducing manufacturing costs to facilitate access to new high-power materials such as SiC.

100 platform researchers provide a triple expertise in substrates, components, and innovative conversion architectures. They rely on a 200 mm and 300 mm microelectronic production line to validate manufacturing processes and accelerate industrial transfers.

Photo credit: V.GUILLY/CEA

Microsystems 200 mm & 300 mm Platform

A world-class R&D facility

Main Activities

- **Sensors**: Nav-grad inertial sensor, microphone, barometric pressure sensor, pMUT/CMUT, gas sensor, bio-sensor
- **Actuators**: haptic feedback, piezo-scanner, piezo-loudspeaker, GHz-range time reference resonator

Key figures

- 14,000 m² space (clean room)
- 150+ research engineers
- 30 patents per year
- 20+ industrial partners
- 6 startup creation

CEA-Leti's teams support the needs of its industrial partners (major groups, small and medium-sized companies, and startups) across all or some stages of development, using bilateral contractors or collaborative projects.
The platform hosts about twenty industrial partners from mobile phone medical, automotive, industry, aeronautics, special and defense markets.

The Microsystems 200 mm and 300 mm platform develops sensors, actuators, RF microsystems (MEMS-RF) and integrated packaging solutions.

The platform's highlyqualified staff, equipment, and international activities make it the world's leading center for high performance microsystems R&D. The objectives of the R&D conducted at the platform are to optimize the actual sensors and actuators, their integration, their reliability while reducing component cost and energy consumption to transfer them to industrial partners. The platform investigates also new materials in particular new piezoelectric material generations, creates, and develops new components with the associated technological channels.

The microsystems platform targets the mobile phone, medical, automotive, industry, aeronautics, spatial and defense markets.

The platform has 20 ongoing strategic partnerships with components and systems manufacturers and end users. Its activities cover the entire component-development chain, from simulation, design, and technology development to demonstrator systems and industrial scale-up. Other activities include advanced morphological and electrical characterization and reliability studies.

Photo credit: P.JAYET/CEA

Integrated Circuits Design Platform

Unique in Europe, a research hub dedicated to the advanced design of integrated circuits, from silicon to packaging

Main Activities

- Digital integrated circuits, multi-core processors
- Analog, RF, and mmW integrated circuits
- Mixed integrated circuits
- Next generation memory circuits
- Neuromorphic circuits, cybersecurity, etc.

Key figures

- 2,500 m²
- 175 researchers
- About 35 patents a year
- Portfolio of 350 patents
- About 80 publications per year
- €22 M cumulated investments
- 50+ industrial partners

Who is the platform for?

- Microelectronics foundries
- Microelectronics fabless companies
- Startups
- Equipment suppliers using integrated circuits
- Software and CAD providers

Collaboration methods:

- Bilateral R&D partnership contracts
- Joint laboratories
- Research programs

The Integrated Circuits Design Platform brings together more than 170 research engineers at the CEA Grenoble site. It develops for its industrial partners advanced digital, analog, mixed-signal and radio-frequency (RF) circuits with innovating architectures, technologies and performances especially in terms of low power consumption.

The IC Design Platform's scope of intervention covers all aspects of design, from silicon substrates to advanced packaging. Relying on foundry technological solutions and services to manufacture its circuits, CEA-Leti resources are used to characterize and validate prototypes as part of its R&D mission to secure and accelerate the subsequent industrialization process.

The platform features state-of-the-art computer-aided design (CAD) software and equipment, enabling design, hardware emulation and electrical characterization. It collaborates with CAD software suppliers to create new products adapted to emerging technologies. The scope of its activities and expertise make it a design center without equal in Europe.

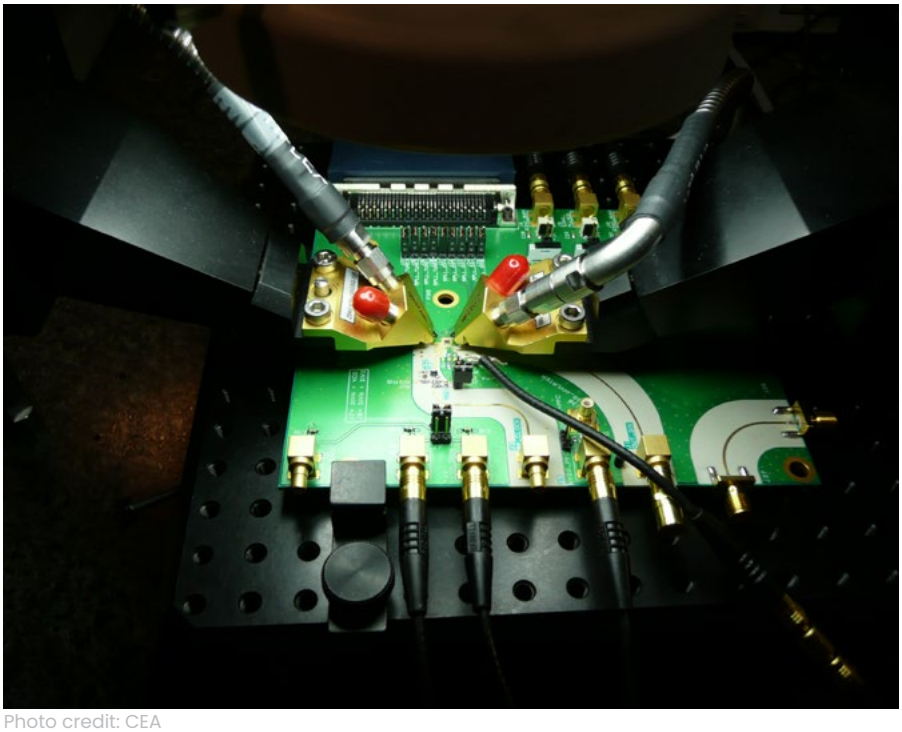


Photo credit: CEA

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Research for industrial innovation